AMENDMENTS TO THE CLAIMS

Claims 1-24 (cancelled)

Claim 25 (new) An analog-to-digital (A/D) converter, comprising:

an input, for receiving a series of analog signals;

an output, for outputting a series of digital signals respectively corresponding to said series of analog signals;

a plurality of A/D cells, each of said A/D cells for converting one of said series of analog signals to a corresponding one of said series of digital signals; and

a control circuit, coupled to said input, said output, and said plurality of A/D cells;

wherein said control circuit operates said input, said output, and said plurality of A/D cells so that each successive A/D cell is assigned, at a different time, to convert a different one of each successive analog signal from said series of analog signals to a corresponding digital signal in said series of digital signals.

Claim 26 (new) The analog-to-digital converter of claim 25, wherein said different time correspond to a different period of a clock signal provided to said analog-to-digital converter.

Claim 27 (new) The analog-to-digital converter of claim 25, wherein each of said A/D cells further comprises a calibration element, said calibration element being set so that each A/D cell coverts the same analog signal present at said input to a same digital value at said output.

Claim 28 (new) The analog-to-digital converter of claim 25, wherein each of said A/D cells further comprises a noise suppression element.

Claim 29 (new) The analog-to-digital converter of claim 28, wherein said noise suppression element comprises a transistor.

Claim 30 (new) The analog-to-digital converter of claim 25, wherein each A/D cell performs an A/D conversion in a same amount of time.

Claim 31 (new) The analog-to-digital converter of claim 25, wherein each A/D cell performs an A/D conversion using successive approximation.

Claim 32 (new) The analog-to-digital converter of claim 25, wherein said control circuit operates to cause said analog-to-digital converter to begin converting a different one of said series of analog signals on each of a series of successive clock signals.

Claim 33 (new) The analog-to-digital converter of claim 33, wherein said control circuit operates to cause said analog-to-digital converter to output a series of digital signals on each of a series of successive clock signals.

Claim 34 (new) A method for converting a series of analog signals to a corresponding series of digital signals, comprising:

receiving over a period of time, a series of analog signals;

assigning each analog signal from said series of analog signals as they are received to an available A/D cell for analog-to-digital conversion to a corresponding digital signal; and

outputting a different digital signal corresponding to a respective analog signal from said series of analog signals as each A/D cell finishes its analog-to-digital conversion;

wherein at least two A/D cells are performing respective analog-to-digital conversions while another A/D cell outputs one of said digital signals.

Claim 35 (new) The method of claim 34, further comprising:

calibrating each A/D cell so that an analog-to-digital conversion performed on a same analog signal by any A/D cell results in a same digital signal.

Claim 36 (new) The method of claim 34, wherein said step of assigning comprises a step of suppressing comparator kickback noise during said analog-to-digital conversion.

Claim 37 (new) The method of claim 34, wherein each A/D cell performs an analog-to-digital conversion in a same amount of time.

Claim 38 (new) The method of claim 34, wherein each A/D cell perform an analog-to-digital conversion using successive approximation.